PATENT APPLICATION

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re the Application of

Simon DELEONIBUS Attn: PCT Branch

Application No. New U.S. National Stage of PCT/FR04/000467

Filed: August 18, 2005 Docket No.: 125073

For: METHOD FOR DELINEATING A CONDUCTING ELEMENT DISPOSED ON AN INSULATING LAYER, DEVICE AND TRANSISTOR THUS OBTAINED

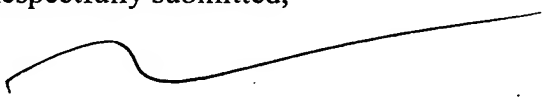
TRANSLATION OF THE ANNEXES TO THE INTERNATIONAL PRELIMINARY EXAMINATION REPORT

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

Attached hereto is a translation of the annexes to the International Preliminary Examination Report (Form PCT/IPEA/409). The attached translated material replaces the claims.

Respectfully submitted,



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Claims

1. Method for delineating a conducting element (1) disposed on an insulating layer (2), comprising deposition of a conducting layer (3) on the front face of the insulating layer (2) disposed on a substrate (4), formation of a mask (5) on at least one area (6) of the conducting layer (3) designed to form the conducting element (1), so as to delineate in the conducting layer at least one complementary area (7) not covered by the mask (5), the complementary areas (7) of the conducting layer (3) being rendered insulating by oxidation, method characterized in that it comprises formation, in said complementary areas (7) of the conducting layer (3), of a volatile oxide from the material of the conducting layer (3) and the oxygen arising from oxidation, the conducting layer (3) evaporating at least partly.

2. Method according to claim 1, characterized in that oxidation is performed before the mask (5) is removed.

3. Method according to claim 1, characterized in that oxidation is performed after the mask (5) has been removed.

4. Method according to any one of the claims 1 to 3, characterized in that formation of the volatile oxide and evaporation of the conducting layer (3) take place during oxidation.

5. Method according to any one of the claims 1 to 3, characterized in that the volatile oxide is formed, after oxidation, by stabilizing and evaporating annealing.

6. Method according to any one of the claims 1 to 5, characterized in that oxidation of the complementary areas (7) of the conducting layer (3) comprises oxygen implantation.

7. Method according to any one of the claims 1 to 5, characterized in that oxidation of the complementary areas (7) of the conducting layer (3) comprises thermal oxidation.

8. Method according to any one of the claims 1 to 7, characterized in that the complementary areas (7) rendered insulating have a thickness at least equal to one atomic layer.

9. Method according to any one of the claims 1 to 8, characterized in that deposition of the conducting layer (3) comprises a first step of deposition of a first conducting layer (3a) and a second step of deposition of a second conducting layer (3b) on the front face of the first conducting layer (3a).

10. Method according to claim 9, characterized in that it comprises etching of the second conducting layer (3b) after formation of the mask (5) and before oxidation.

11. Method according to one of the claims 9 and 10, characterized in that the material of the first conducting layer (3a) is taken from the group comprising

tungsten, molybdenum, nickel and cobalt, and the material of the second conducting layer (3b) is polycrystalline silicon.

12. Device comprising a conducting element (1) disposed on an insulating layer (2), characterized in that it is obtained by the method according to any one of the claims 9 to 11, the area (6b) of the second conducting layer (3b), designed to form the conducting element (1), being salient at the periphery of the area (6a) of the first conducting layer (3a).

13. Transistor comprising a gate electrode, characterized in that the gate electrode is achieved by the method according to any one of the claims 1 to 12.